

FIG. 1

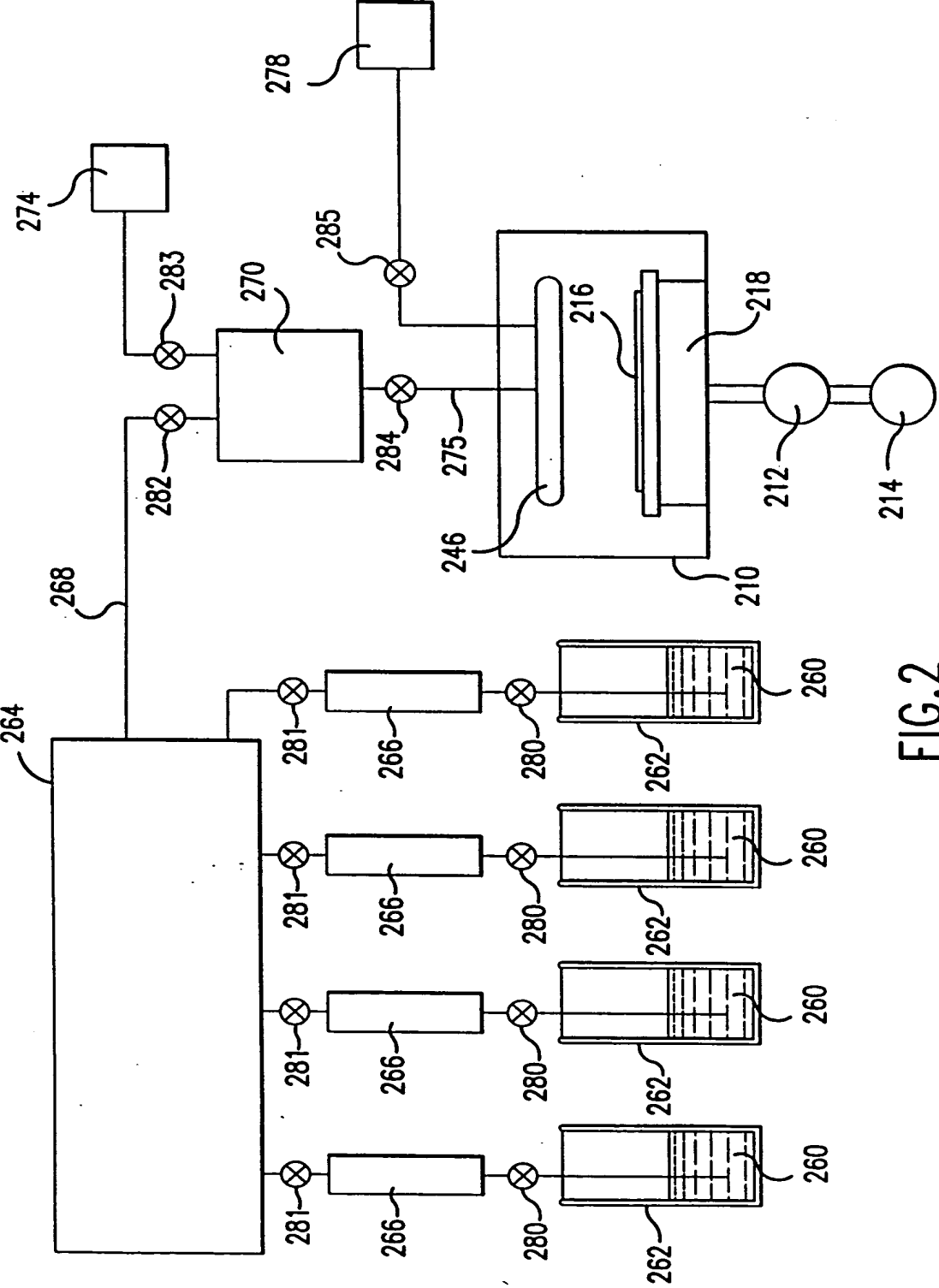


FIG. 2

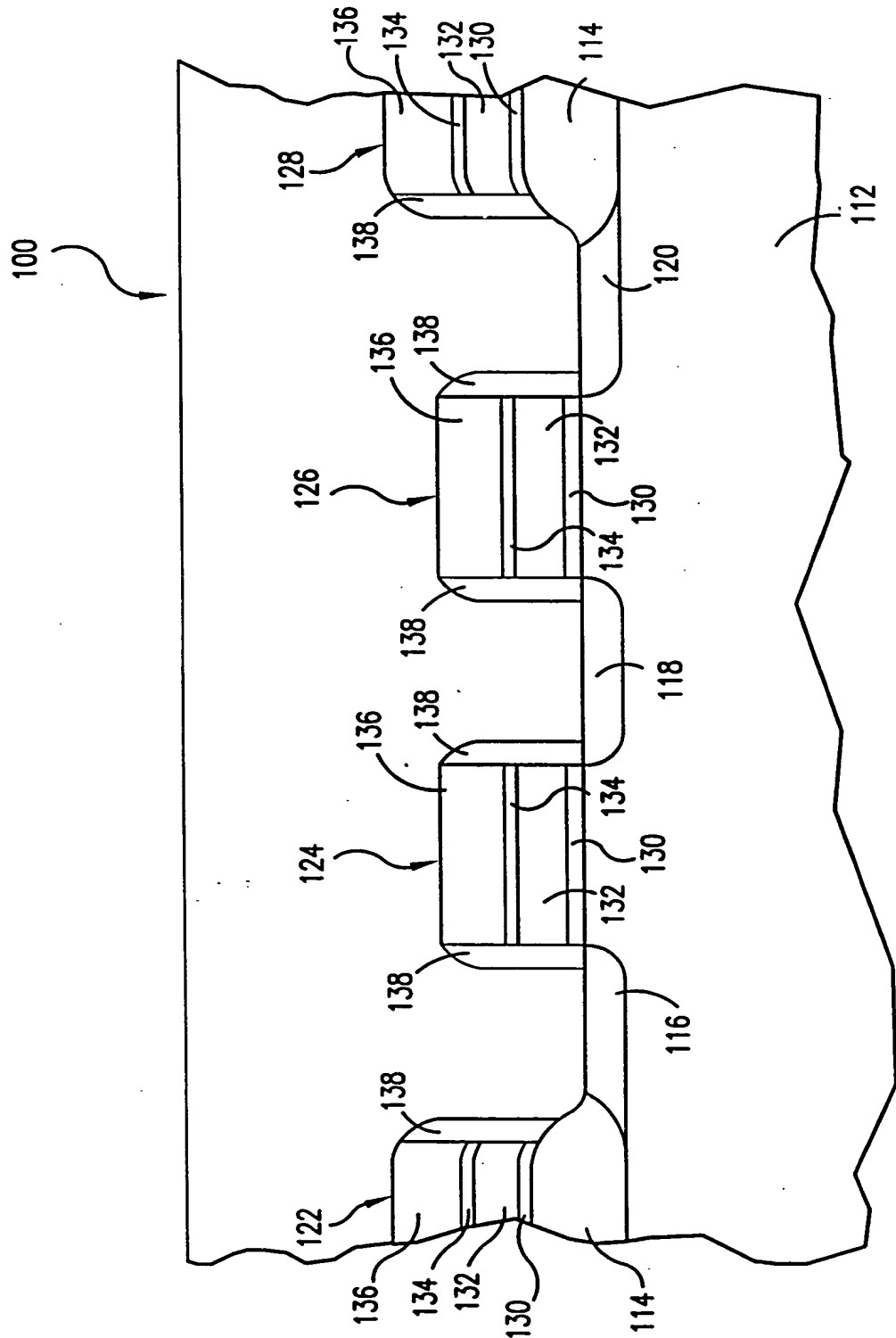
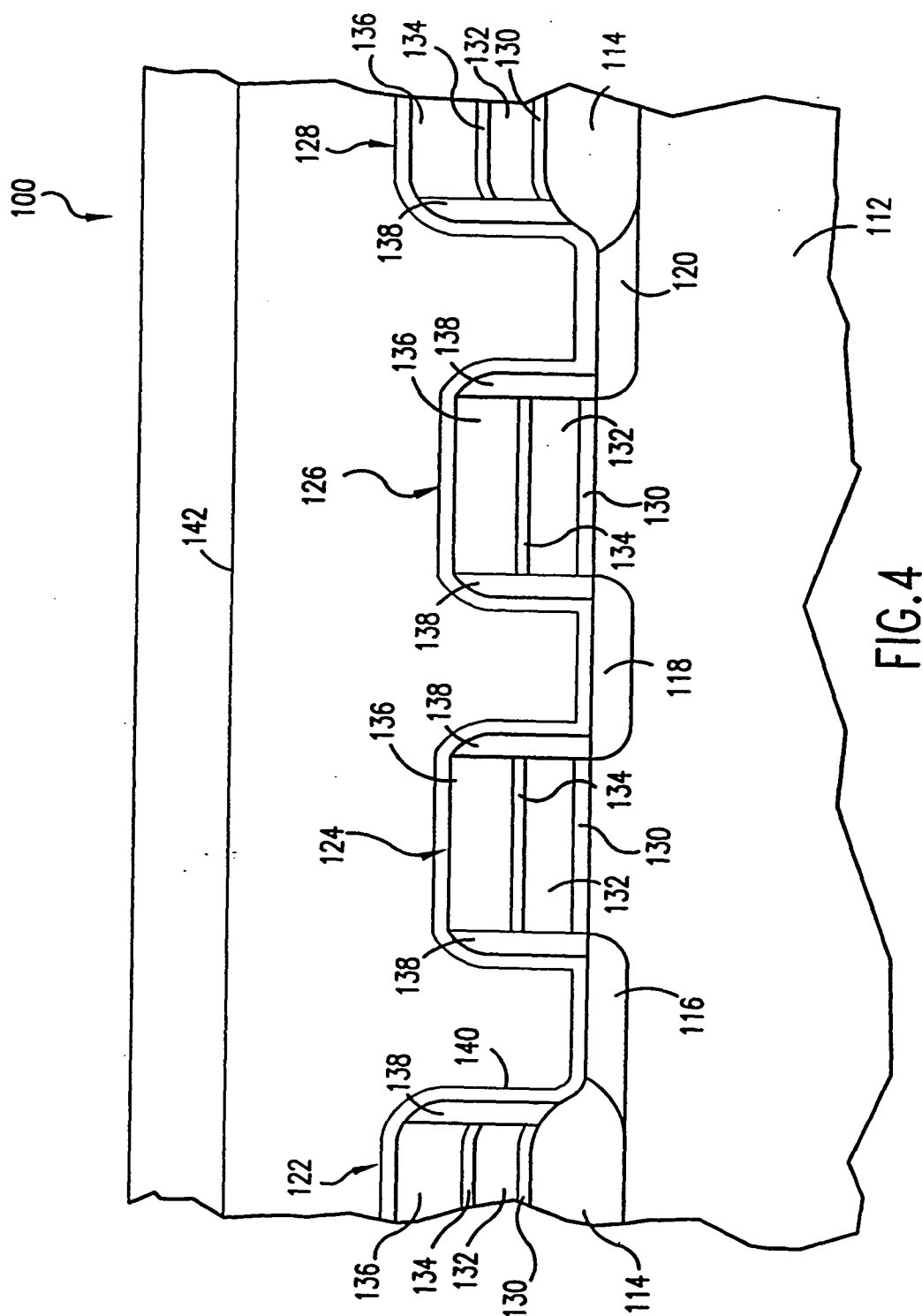
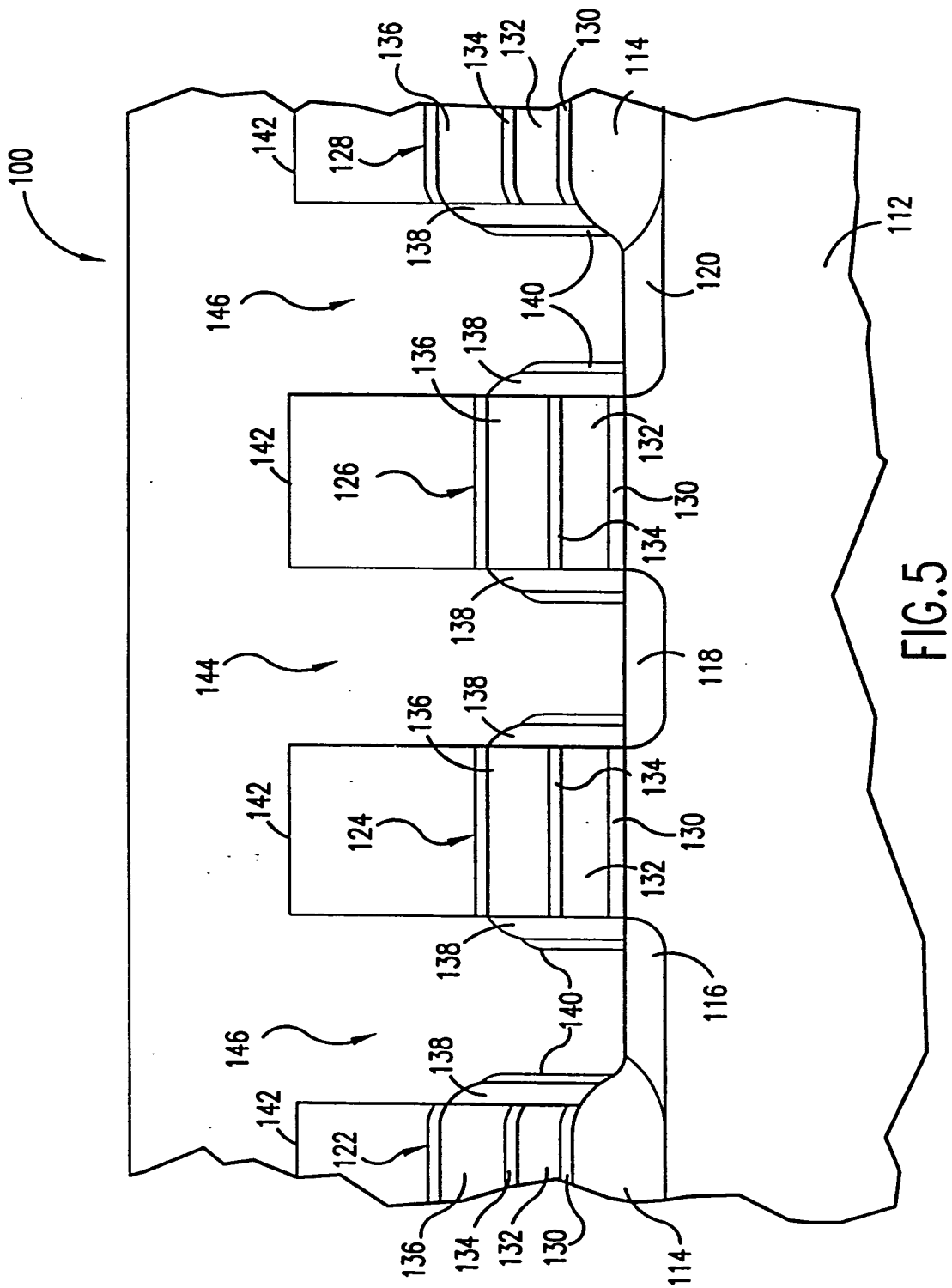
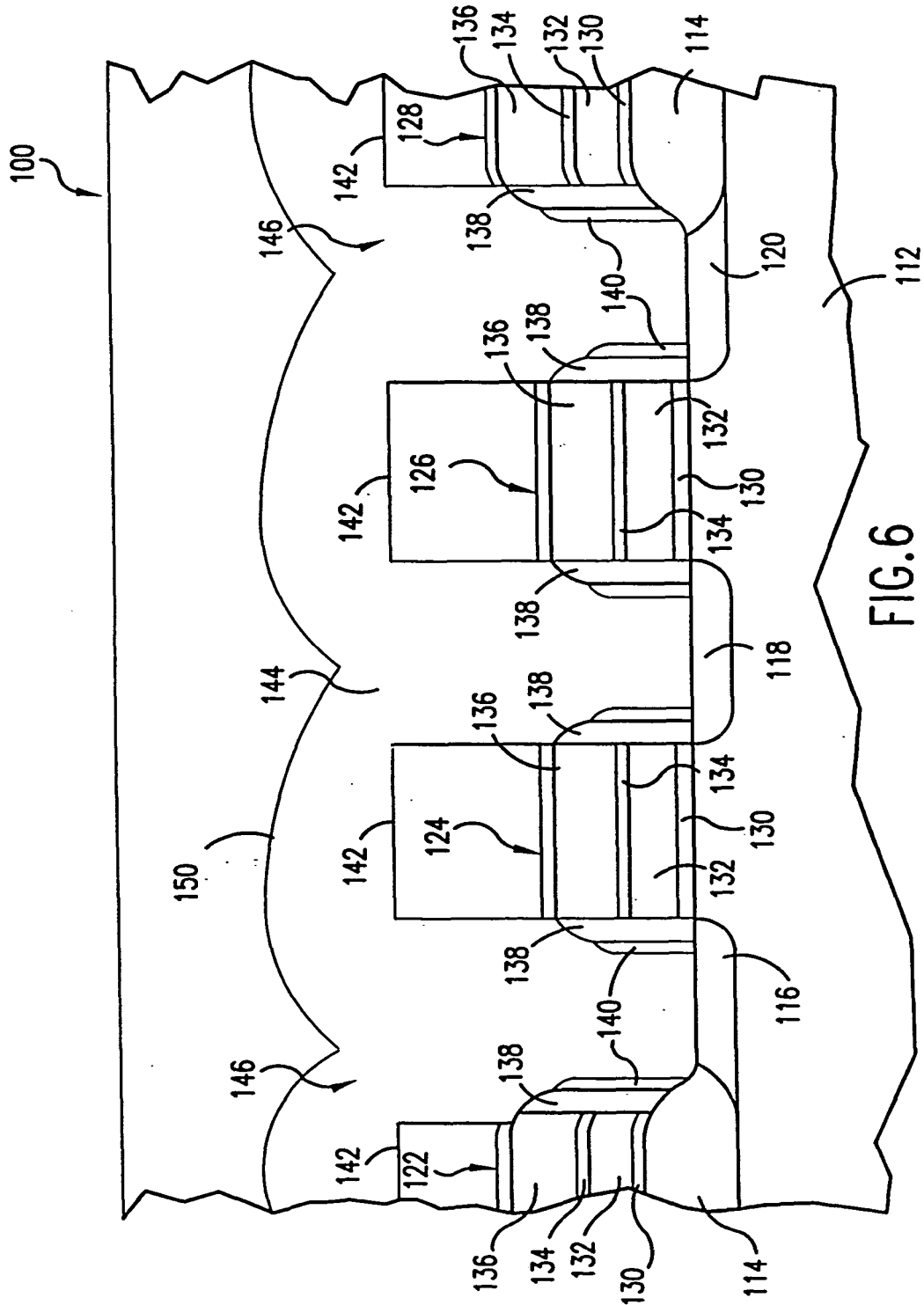
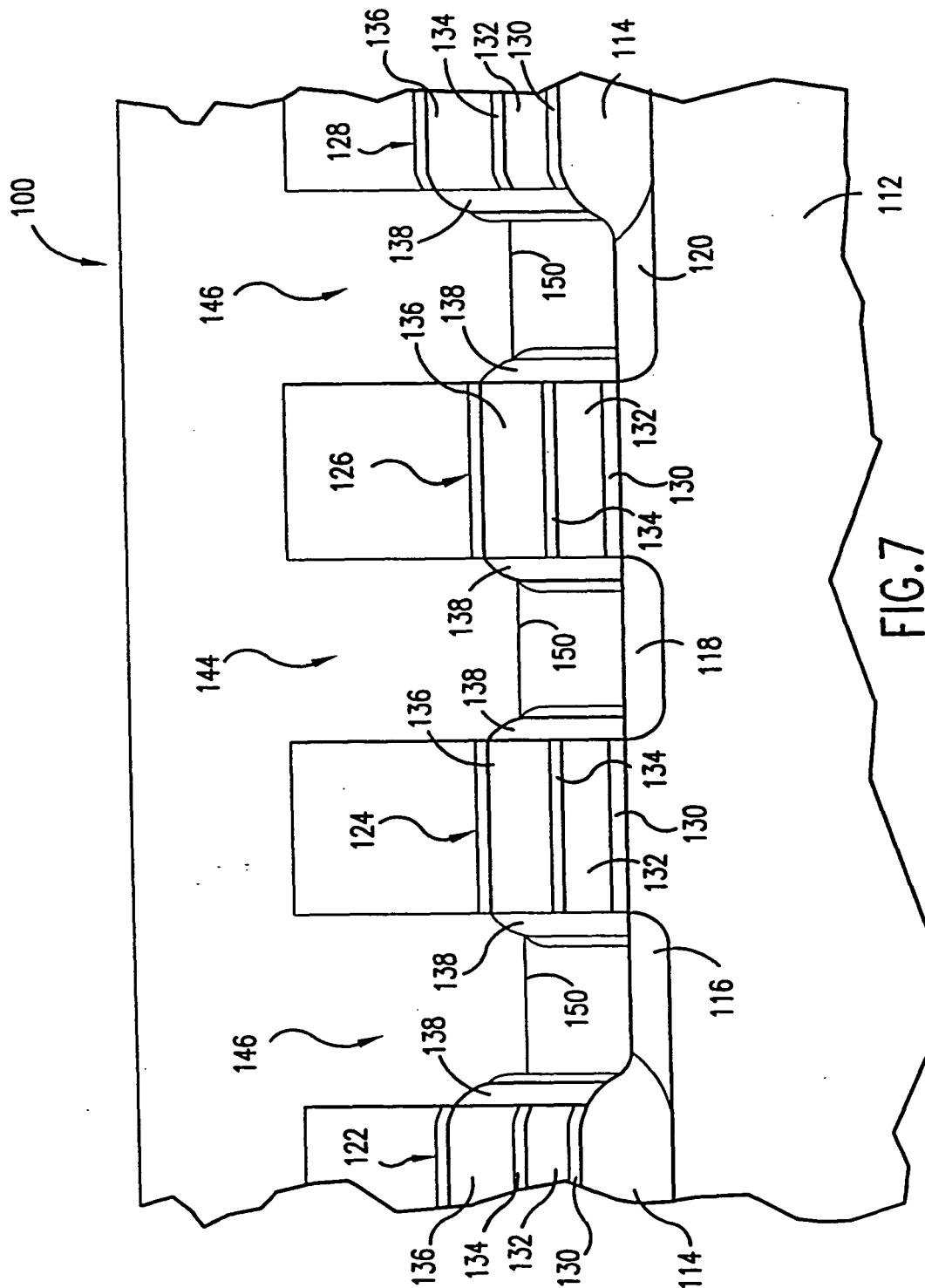


FIG.3









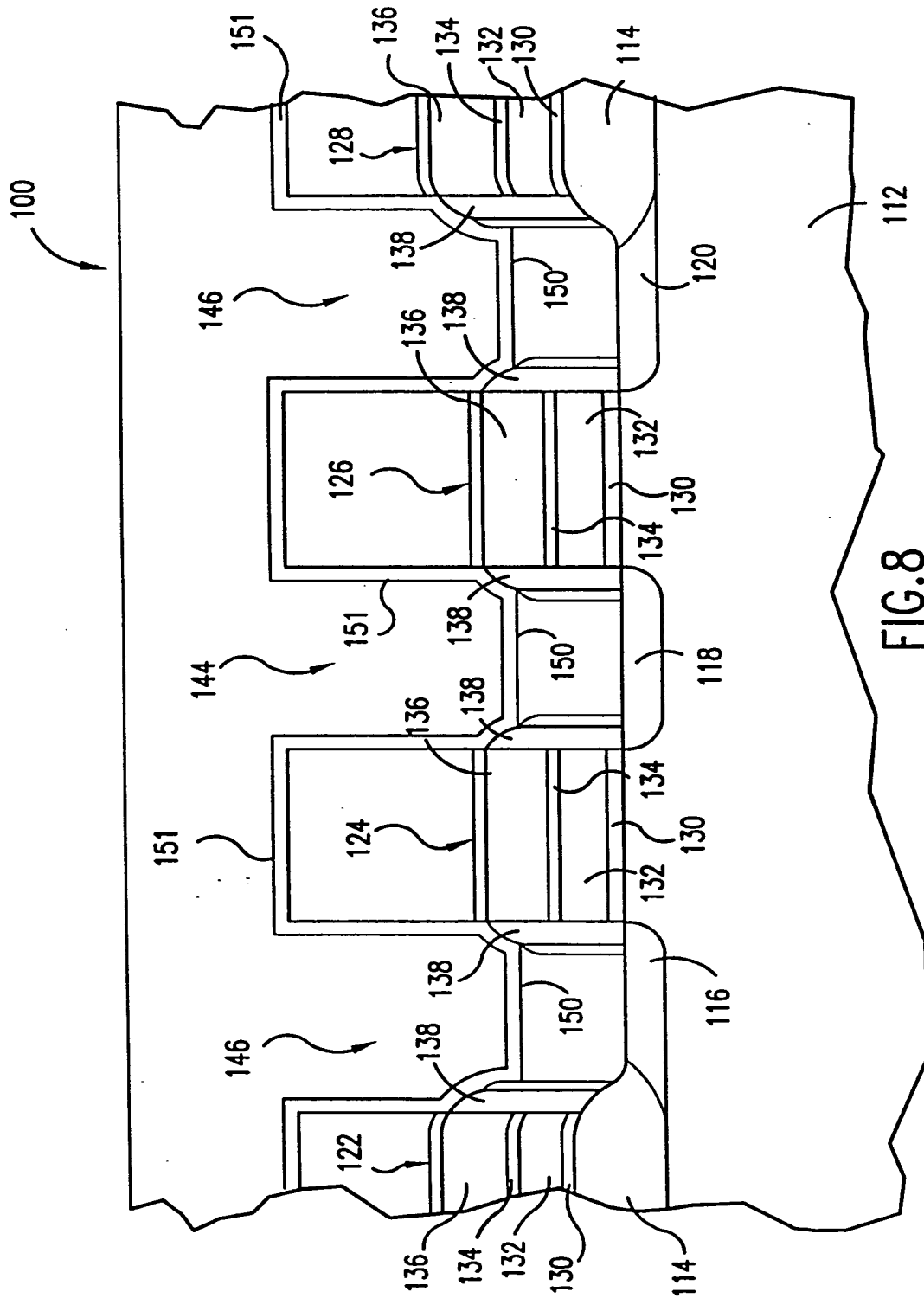


FIG.8

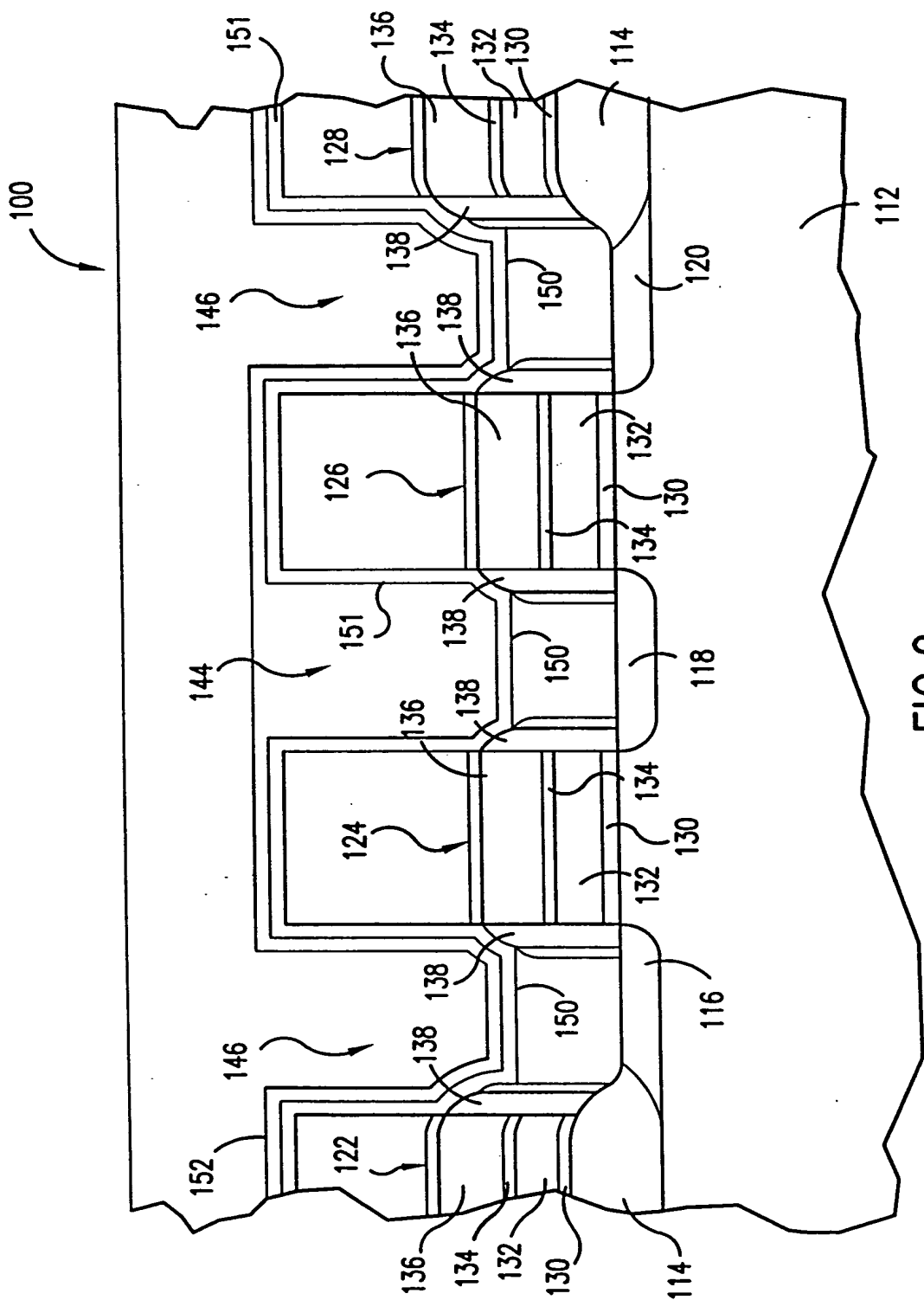


FIG.9

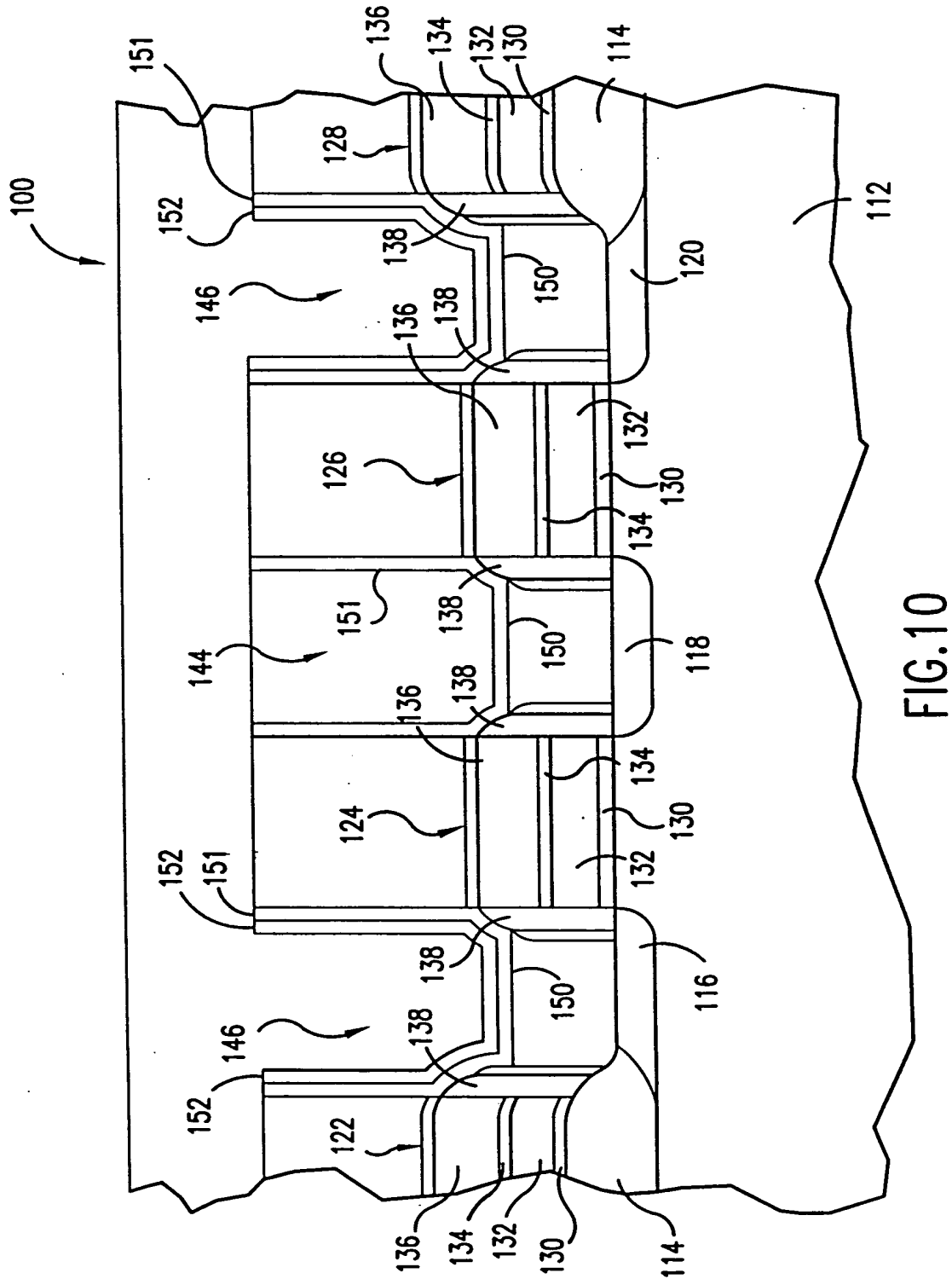


FIG.10

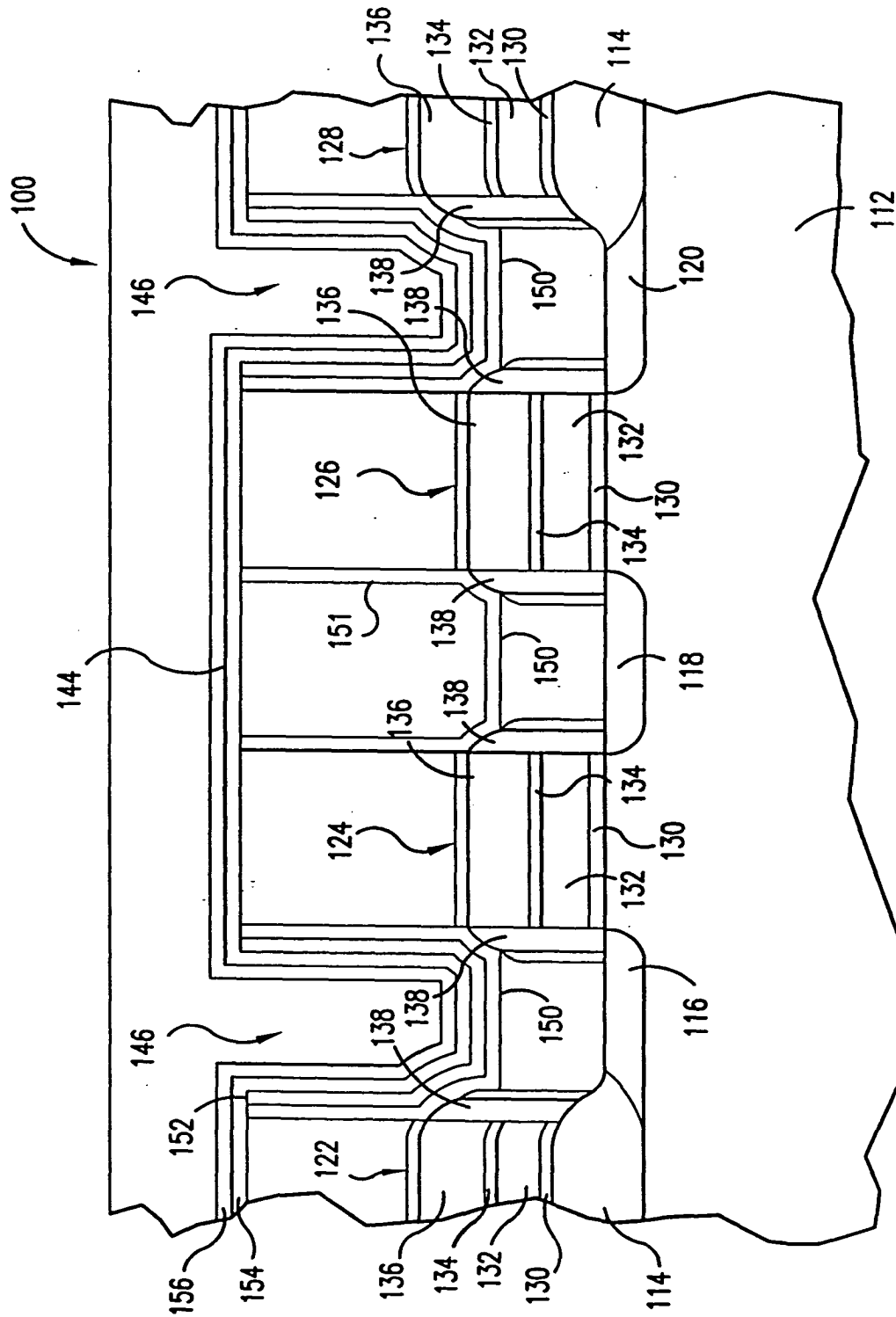


FIG.11

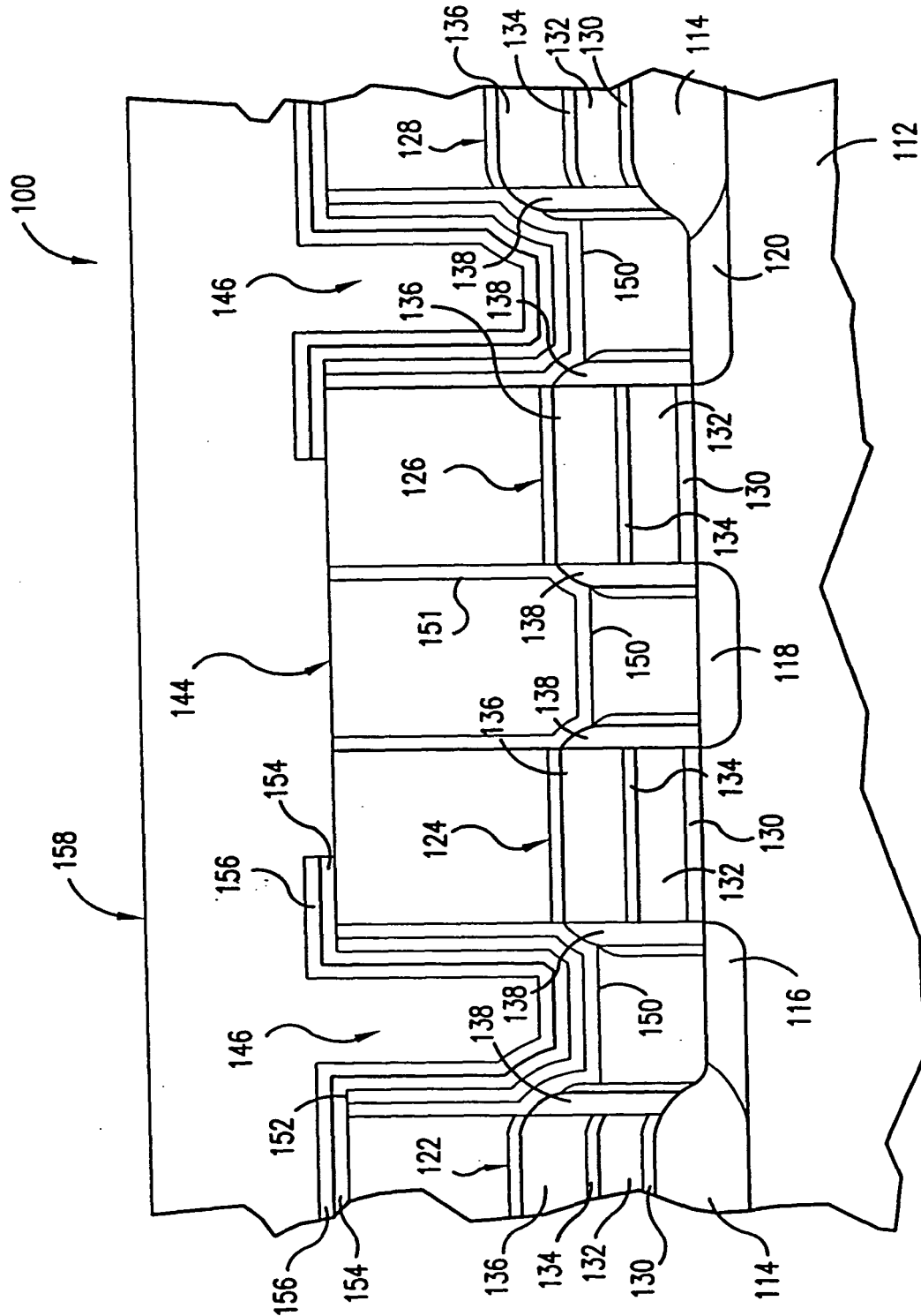


FIG.12



App No.: Not Yet Assigned Docket No.: M4065.0133/P133-B
Inventor: Brian A. Vaartstra, et al.
Title: METHOD OF FORMING BARRIER LAYERS (AS
AMENDED)

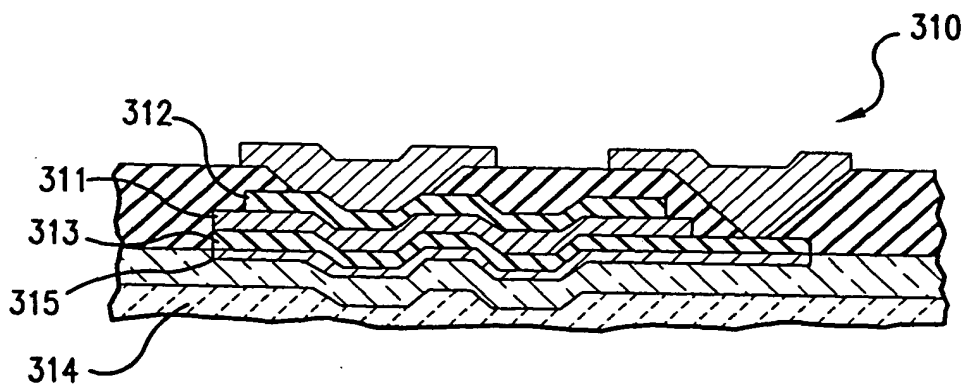


FIG.14

This cross-sectional view shows a semiconductor device with a central channel region 424. The device is surrounded by a substrate 416 and a passivation layer 438. Various layers are labeled with reference numerals 428, 430, 432, 434, and 436. The source and drain regions are labeled 420 and 422, and the gate regions are labeled 426. The device is shown in a cross-sectional view, with the substrate 416 at the bottom and the passivation layer 438 at the top. The channel region 424 is located between the source and drain regions 420 and 422. The gate regions 426 are located above the channel region 424. The layers 428, 430, 432, 434, and 436 are shown as different regions within the device structure.

FIG. 15

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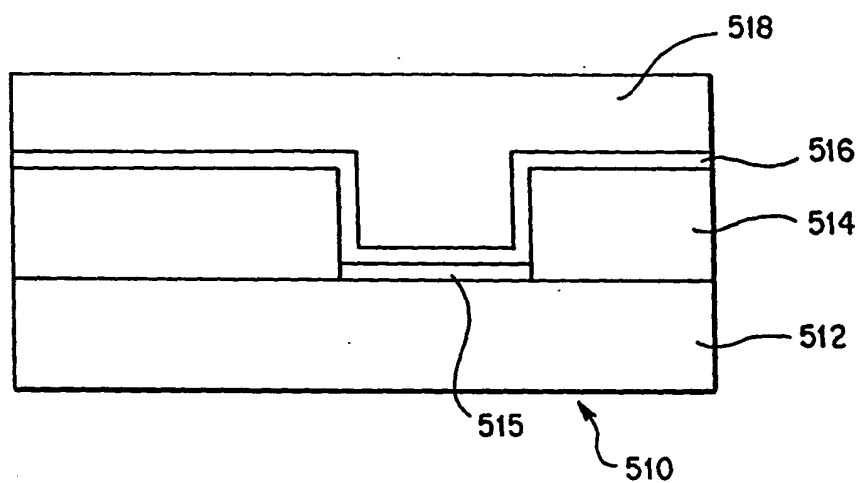


FIG.16

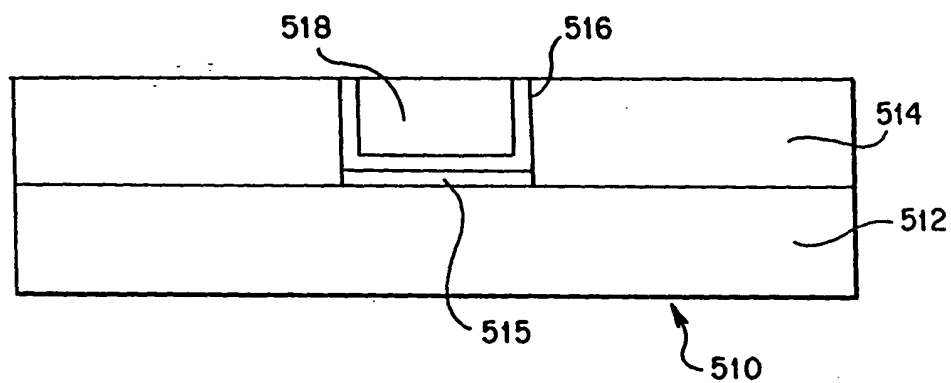


FIG.17